between adjacent substrates, a non-polymeric bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof.

89. (Amended) The apparatus of claim 88, further comprising vertical interconnects having vertical interconnect segments formed of a first metal contact on a first substrate bonded to a second aligned metal contact on a second adjacent substrate.

90. (Amended) The apparatus of claim 89, wherein the plurality of aligned vertical interconnect segments are joined to form a vertical interconnect between non-adjacent substrates.

101. (Amended) A stacked integrated circuit comprising:

a plurality of integrated circuit substrates having formed on corresponding surfaces thereof complementary patterns of a material bondable using thermal diffusion bonding; and

a thermal diffusion bonded region between the complementary patterns.

Please add new claims 102-117 as follows:

102. (New) The apparatus of claim 101, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has memory circuitry formed thereon, the memory circuitry having a plurality of memory locations including at least one memory location used for sparing, wherein data from the at least one memory location on the at least one integrated circuit substrate that has memory circuitry formed thereon is used instead of data from a defective memory location on the at least one integrated circuit substrate that has memory circuitry formed thereon.

103. (New) The apparatus of claim 101, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has memory circuitry formed thereon and at least one integrated circuit substrate of the plurality of integrated circuit substrates has logic circuitry formed thereon, wherein the at least one integrated circuit substrate that has logic circuitry formed thereon performs programmable gate line address assignment with

respect to the at least one integrated circuit substrate that has memory circuitry formed thereon.

104. (New) The apparatus of claim 101, wherein information processing is performed on data routed between circuitry of at least two of the plurality of integrated circuit substrates.

105. (New) The apparatus of claim 101, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has reconfiguration circuitry.

106. (New) The apparatus of claim 101, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has logic circuitry formed thereon for performing at least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

107. (New) The apparatus of claim 101, further comprising:

a memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores a data value and has circuitry for coupling that data value to one of the plurality of data lines in response to receiving a gate control signal from one of the plurality of gate lines;

circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and

a controller that determines if one of the plurality of memory cells is defective and alters the mapping to eliminate references to the one of the plurality of memory cells that is defective.

108. (New) The apparatus of claim 101, further comprising:

at least one controller substrate having logic circuitry formed thereon;

at least one memory substrate having memory circuitry formed thereon;

a plurality of data lines and a plurality of gate lines on each memory substrate;

an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting of one of the plurality of gate lines;

a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and

controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

109. (New) The apparatus of claim 108, wherein said controller substrate logic:

tests the array of memory cells periodically to determine if one of said memory cells is defective; and

removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

110. (New) The apparatus of claim 108, further comprising programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

111. (New) The apparatus of claim 108, wherein the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order, wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

112. (New) The apparatus of claim 108, wherein:

the logic circuitry of the at least one controller substrate is tested by an external means; and

the array of memory cells of the at least one memory substrate are tested by the logic circuitry of the at least one controller substrate, wherein the testing achieves a functional testing of a substantial portion of the array of memory cells.

113. (New) The apparatus of claim 108, wherein the logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

114. (New) The apparatus of claim 108, wherein the controller substrate logic is further configured to:

prevent the use of at least one defective gate line; and

replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

115. (New) The apparatus of claim 108, wherein the controller substrate logic is further configured to prevent the use of at least one defective gate line.

116. (New) The apparatus of claim 108, wherein the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate.

117. (New) The apparatus of claim 101, wherein at least one of the plurality of integrated circuit substrates is a thinned substantially flexible substrate.